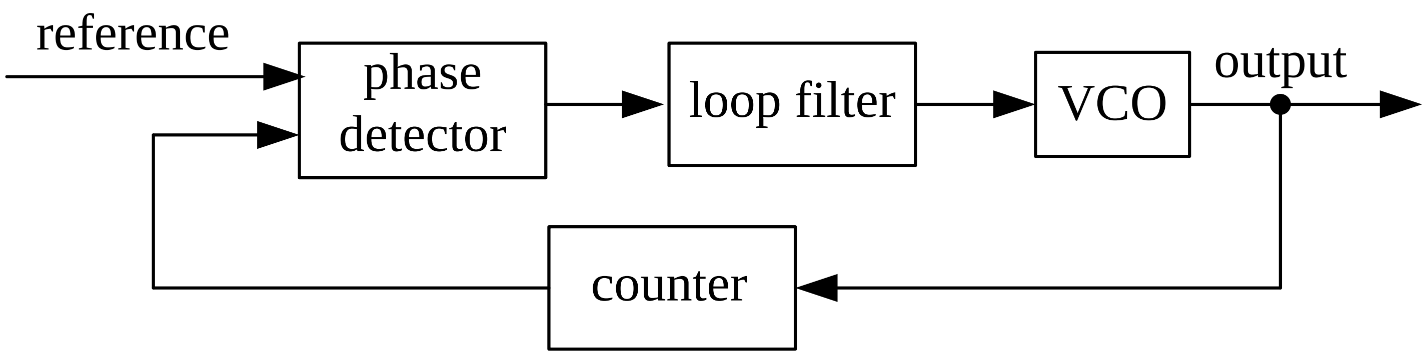
Phase Locked Loop



The simplest PLL structure is based on a phase detector, a low-pass filter and a voltage-controlled oscillator (VCO). This structure, widely used in hardware realizations, can be classified as a zero-crossing structure in which the detection of phase and frequency is based on the zero crossing points of the input signal. The dynamic performances of this solution are limited as the zero crossing points are only detected at every half-cycle of the utility frequency. Moreover, the noise around the zero-voltage crossing point makes the output angle oscillate.

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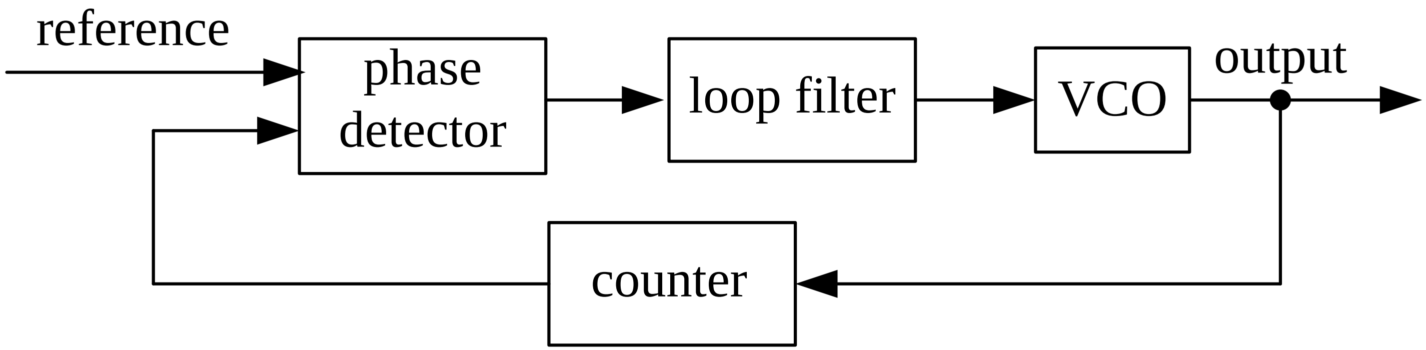

The difference between phase angle of the input and that of the output signal is measured by the PD and passed through the LF. The LF output signal drives the voltage-controlled oscillator (VCO) to generate the output signal.

The PD multiplies its inputs to generate a signal which has a low-frequency component. This component is proportional to, or at least a monotonic function of, the phase difference. The LF filters high-frequency components and provides a proper error signal which is used by the VCO as a measure of variations of the phase. Any change in the phase angle (or frequency) of the input signal causes deviation of the error signal from zero and the control loop regulates it again to zero by introducing proper variations in the frequency of the VCO..

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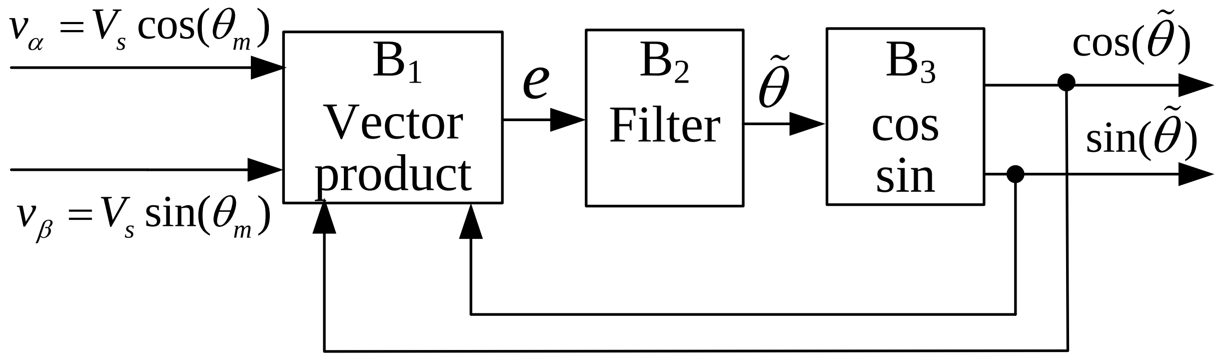

A different solution, more convenient for software realizations, employs a closed-loop system in which the error signal is obtained by the comparison between a measured grid waveform and the obtained one. This solution is rather appropriate in three-phase systems allowing the determination of the error signal by a vector product.

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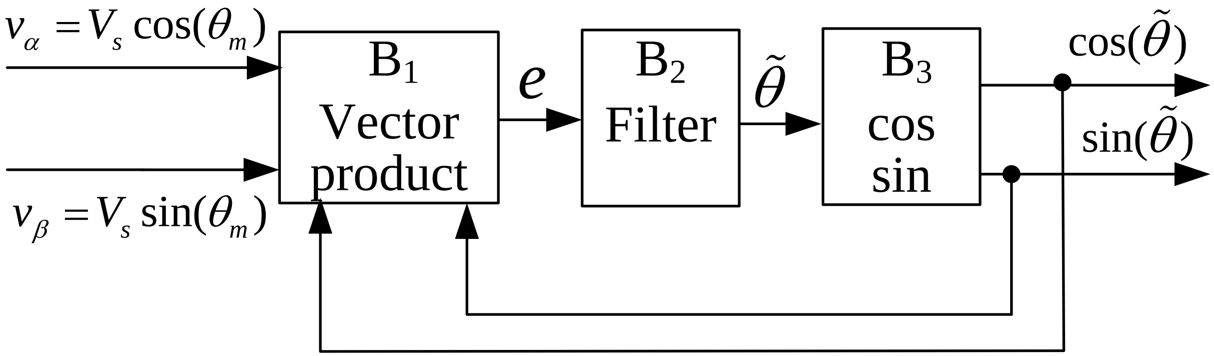

system based on the vector product between the components of the measured grid voltage phasor and the estimated values of the sine and cosine of the grid angle .
The PLL structure is essentially composed by three blocks.
Block B_1 achieves the vector product and generates signal error *e*. In particular signal error *e* is approximated by its sine and it is obtained as:

$$e \cong \sin(\theta_m - \tilde{\theta}) = \frac{v_\beta \cos(\tilde{\theta}) - v_\alpha \sin(\tilde{\theta})}{V_s} =$$

$$= \sin(\theta_m)\cos(\tilde{\theta}) - \cos(\theta_m)\sin(\tilde{\theta}),$$

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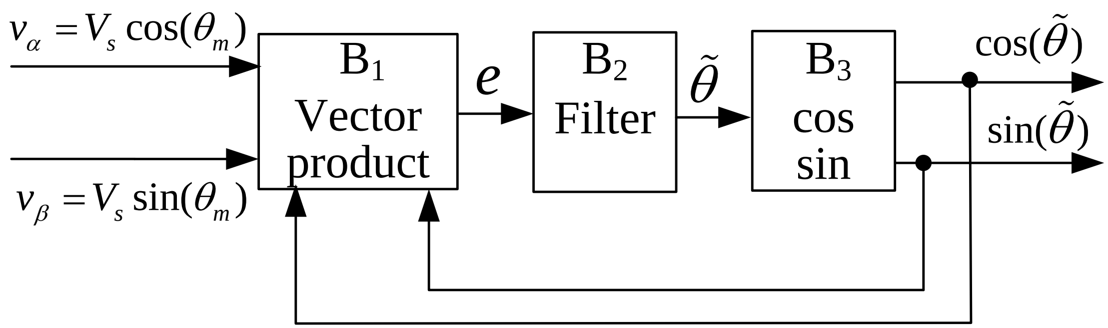

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$$= \sin(\theta_m)\cos(\tilde{\theta}) - \cos(\theta_m)\sin(\tilde{\theta}),$$

where vα and vβ are the components of the grid voltage phasor, referred to a fix reference frame α and β, Vs and   are the module and the phase of the grid voltage phasor and sin($\tilde{\theta}$) and cos($\tilde{\theta}$) are the sine and the cosine of estimated grid angle provided by the PLL system Block B2 is the loop filter that performs the estimation of the phase angle of the grid voltage phasor.

Block B3 determines the values of the sine and cosine of phase angle this can be achieved employing a numerical procedure or through tables.

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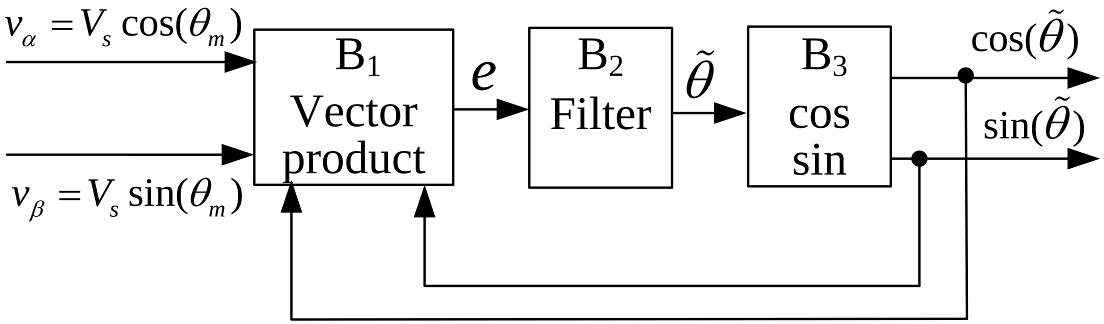

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The loop filter is generally constituted by a Proportional Integral (PI) regulator, providing the estimated value of angular frequency , followed by an integrator, which furnishes the estimation of the grid angle.

The PLL system based on the vector product has a non-linear behaviour; however, for low values of the grid angle error *e*, it is possible to linearly approximate the vector product with the error.

Phase Locked Loop

Using such approach, the open loop transfer function G(s) of the PLL system is equal to:

$$G(s) = K_p \frac{1 + s\tau_I}{s^2 \tau_I},$$

being and respectively the proportional gain and the integral time constant of PI regulator. Therefore, the closed loop transfer function W(s) of the PLL system

$$W(s) = \frac{K_p}{\tau_I} \frac{1 + s\tau_I}{s^2 + K_p s + \frac{K_p}{\tau_I}},$$

has two poles whose position depends on the PI regulator parameters. Imposing complex conjugated poles, with natural frequency and phase :

$$p_{1,2} = -\omega_n \left(\cos(\phi) \pm j \sin(\phi) \right),$$

the following values for the PI regulator parameters are obtained:

$$K_p = 2\omega_n \cos(\phi) \qquad \tau_I = \frac{K_p}{\omega_n^2}.$$

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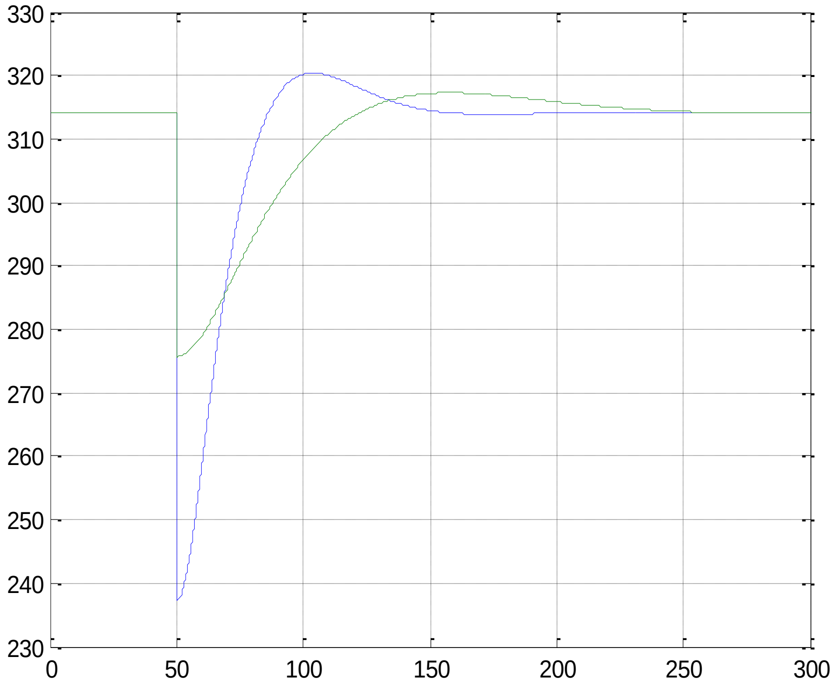
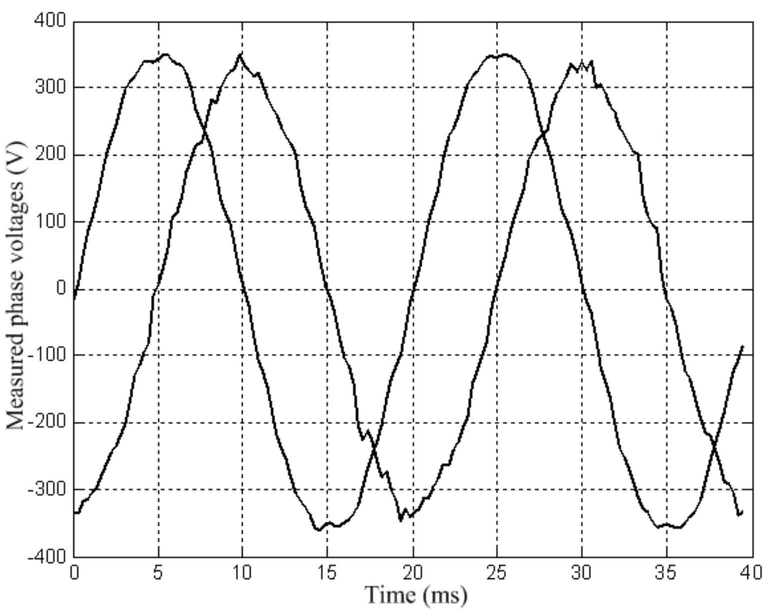


Il comportamento della PLL con regolatore PI è in genere soddisfacente per mantenere un aggancio di fase negli alimentatori UPS in quanto in tali sistemi l'aggancio di fase successivo ad un salto di fase della rete può avvenire in tempi relativamente lunghi. Nei sistemi di alimentazione connessi alla rete, invece, quando si verifica un salto di fase della rete occorre che l'aggancio di fase sia nettamente più rapido.

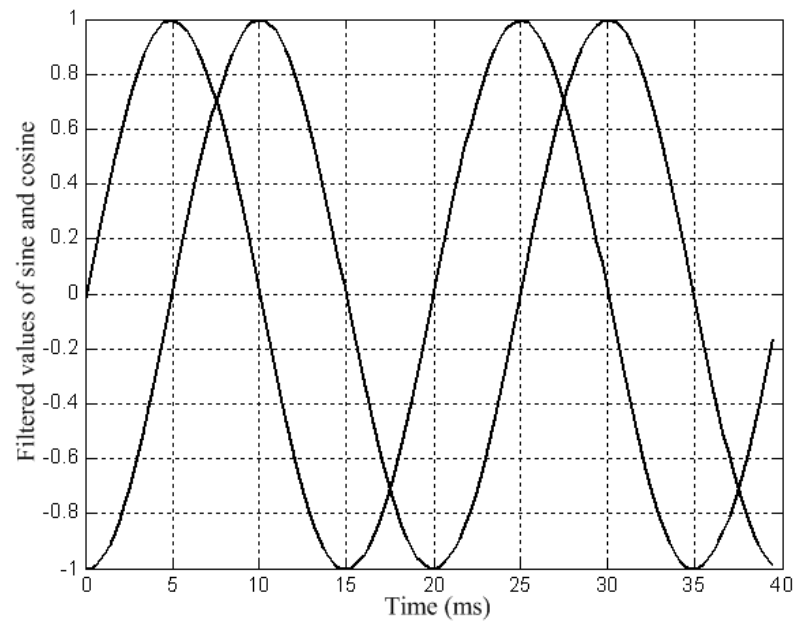
Questa esigenza comporta la scelta di una pulsazione naturale   dell'ordine di qualche decina di rad/s e, di conseguenza, anche il coefficiente deve essere dell'ordine di alcune decine.   Quando si verifica il salto di fase, la pulsazione determinata dalla PLL subisce un salto pari al valore del coefficiente moltiplicato per il seno dell'angolo corrispondente al salto di fase, come mostrato dalla figura; in essa la curva a tratto continuo riporta l'andamento della pulsazione determinata dal PLL system in corrispondenza ad un salto di fase in anticipo di 60°, avendo scelto i parametri del PI regulator con pulsazione naturale pari a 20 π (10 Hz) e una fase pari a 45°.

Experimental Results

Different experimental tests of the proposed filter were performed on an electronic board, based on a Texas Instruments TMS320F2401 DSP, connecting a three phase inverter prototype to a 50 Hz 380V utility grid.



Measured phase voltages v_α and v_β.



Shapes of sine and cosine output by the filter.

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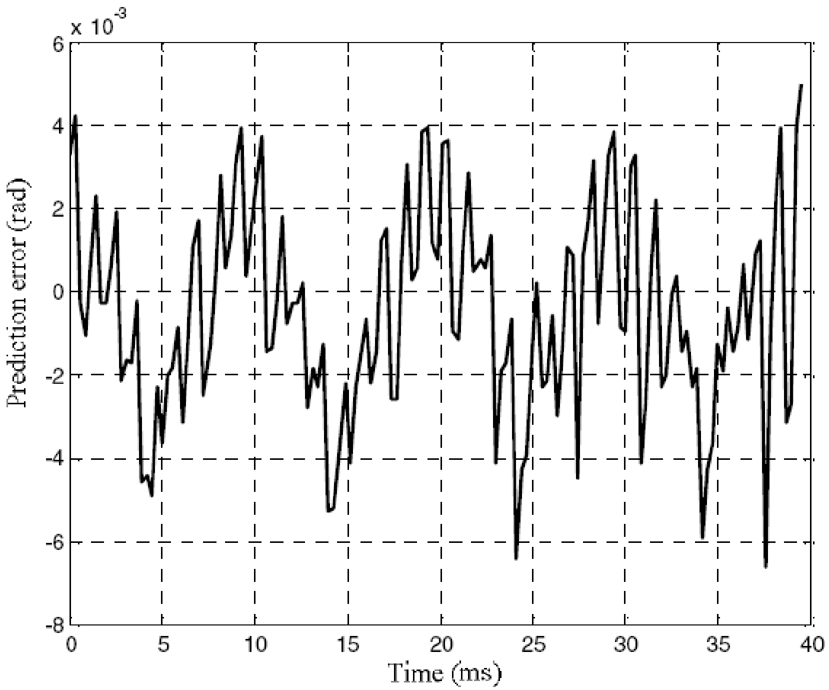

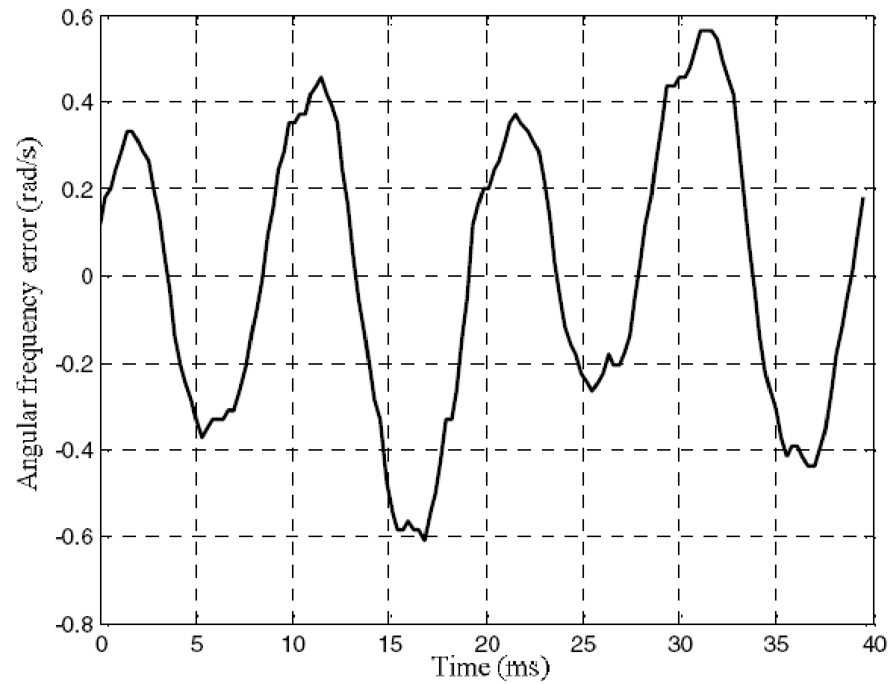

Single-phase PLL

Nel caso monofase è possibile utilizzare lo stesso approccio del caso trifase pur di anteporre al sistema una opportuna funzione in grado di generare un segnale in quadratura con la tensione misurata dalla rete.